pulsewidth modulation circuitry for generating pulsewidth modulated video data; and

a1 cancel

driver circuitry for latching the pulsewidth modulated video data and driving said signal lines in accordance with the latched data.

9. (Amended) A matrix type display device comprising:

display elements connected to row lines and column lines; and

a driver circuit for driving said column lines, said driver circuit comprising:

a2

pulsewidth modulation circuitry for generating pulsewidth modulated video data; and

driver circuitry for latching the pulsewidth modulated video data and driving said column lines in accordance with the latched data.

18. (Amended) A method of driving signal lines of a matrix type display device, comprising:

a3

generating pulsewidth modulated video data;

latching the pulsewidth modulated video data; and

driving said signal lines in accordance with the latched data.

Please add the following new claims 22-25:

--22. A driver circuit for driving signal lines of a matrix type display device, comprising:

a4 cont

pulsewidth modulation circuitry for generating pulsewidth modulated video data; and

driver circuitry including latch circuits for latching the pulsewidth modulated video data and output transistors for driving said signal lines in accordance with the latched data.

23. The driver circuit according to claim 22, wherein a single latch circuit is provided for each signal line.

24. The driver circuit according to claim 22, wherein said driver circuitry further includes a data buffer whose outputs are selectively latched into said latch circuits in accordance with latch enable signals.

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25. The driver circuit according to claim 22, wherein said output transistors include series-connected N-channel and P-channel transistors associated with each signal line, wherein an output of a corresponding latch circuit is supplied to a control terminal of one of the N-channel and P-channel transistors.—

REMARKS

Reconsideration and allowance of the subject patent application are respectfully requested.

Claims 1, 2, 5, 6, 8-11, 15, 17-19 and 21 were rejected under 35 U.S.C. Section 102(e) as allegedly being anticipated by Sakuragi *et al.* (U.S. Patent No. 6,195,076). A